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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ANANTHANARAYANAN, RAMYA	
ART UNIT	**PAPER NUMBER**
2131	

DATE MAILED: 04/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,601	HEPLER, EDWARD L.	
	Examiner	Art Unit	
	Ramya Ananthanarayanan	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-12 have been examined.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 2, 4, 6, and 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Naruse (U.S. Patent 6,115,410).

4. With respect to claim 2, Naruse discloses a code generator for generating individual binary codes of a set of binary codes, each binary code having 2^M bits;

A counter sequentially outputting M-bit counts in a parallel orientation, each successive count being incremented by 1 (column 5, lines 51-56);

An index selector for outputting an M-bit code identifier in a parallel orientation (column 5, lines 51-56);

A parallel array of M logical gates, each having an output and a first input being one parallel bit from said counter and a second input being one parallel bit from said index selector (column 5, lines 59-67); and

A reduction network of logical gates associated with the outputs of said parallel array of logical gates for outputting a single code bit each time a parallel M-bit count is input to said parallel logical gate array from said counter, such that the binary code which is identified by the M-bit code identifier is produced after 2^M iterations (column 5, lines 59-67).

5. With respect to claim 4, Naruse discloses a system for generating a desired pseudorandom code comprising:

A binary counter for providing a plurality of M-bit sequential binary numbers (column 5, lines 51-56);

An index selector, for outputting an M-bit code identifier of the desired pseudorandom code (column 5, lines 51-56);

At least M logical gates, each having a first input from the binary counter and a second input from the index selector, and each having an output (column 5, lines 59-67); and

An XOR tree for XORing said outputs to provide an XORed output; whereby the desired pseudorandom code is output from said XORed output (Figure 4).

6. With respect to claim 6, Naruse discloses a code generator for generating an individual binary code from a set of N binary codes, each binary code having M bits;

A counter sequentially outputting M-bit binary numbers, each successive binary number being incremented by 1 (column 5, lines 51-56);

An index selector for outputting an M-bit code (column 5, lines 51-56);

A logical gate array having a first input from said counter and a second input from said index selector, and having an output (column 5, lines 59-67);

A reduction network of logical gates associated with the output of said logical gate array for outputting a single code bit each time an M-bit binary number is input to said logical gate array from said counter, such that the binary code identified by the M-bit code is produced after 2^M iterations (column 5, lines 59-67).

7. With respect to claim 9, Naruse discloses a system for generating a desired pseudorandom code comprising:

A binary number generator for providing a binary count comprising a plurality of M-bit binary numbers (column 5, lines 51-56);

An index selector, for providing an M-bit binary identification of said desired pseudorandom code (column 5, lines 51-56); and

A logical reduction means having a first input from the counter and a second input from the index selector and having an output; whereby said desired pseudorandom code is output from said output (column 5, lines 59-67).

8. With respect to claim 10, Naruse discloses a code generator for generating individual binary codes of a set of binary codes, each having 2^M bits;

A binary number generator for outputting a plurality of M-bit binary numbers, each successive binary number being one of a predetermined sequence (column 1, lines 47-65; column 5, lines 51-56);

An index selector for outputting an M-bit code identifier (column 5, lines 51-56);

A parallel array of M logical gates, each having an output and a first input being one bit from said binary number and a second input being one bit from said code identifier (column 5, lines 59-67); and

A reduction network of logical gates associated with the outputs of said parallel array of logical gates for outputting a single code bit each time a binary number is input to said parallel logical gate array from said counter, such that the binary code which is identified by the M-bit code identifier is produced after 2^M iterations (column 5, lines 59-67).

9. With respect to claim 11, Naruse discloses a code generator, whereby said predetermined sequence is a sequence of binary numbers, each binary number being incremented by one over a prior binary number (column 1, lines 47-65).

10. With respect to claim 12, Naruse discloses a system for generating a desired OVSF code comprising:

A binary number generator counter for providing a predetermined sequence of M-bit binary numbers (column 1, lines 47-65; column 5, lines 51-56);

An index selector, for outputting an M-bit code identifier of the desired OVSF code (column 5, lines 51-56);

At least M logical gates, each having a first input from the binary number generator and a second input from the index selector, and each having an output (column 5, lines 59-67); and

An XOR tree for XORing said outputs to provide an XORed output; whereby the desired OVSF code is output from said XORed output (Figure 4).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1, 3, 5, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naruse (U.S. Patent 6,115,410) in view of Chan (U.S. Patent 6,262,751).

13. Naruse and Chan are analogous art because both solve the problem of orthogonality in data to be processed.

14. With respect to claim 1, Naruse discloses a system for generating an OVSF code comprising:

A binary counter for providing a binary count comprising a plurality of sequential M-bit binary numbers (column 5, lines 51-56);

An index selector, for providing an M-bit binary identification of said OVSF code (column 5, lines 51-56); and

A logical reduction means having a first input from the counter and a second input from the index selector and having an output; whereby the desired OVSF code is output from said output (column 5, lines 59-67).

15. Naruse does not disclose a system comprising:

Bit reordering means, for selectively reordering the bits of each said binary number from least significant bit to most significant bit.

Chan discloses a system comprising:

Bit reordering means, for selectively reordering the bits of each said binary number from least significant bit to most significant bit (Figure 10).

16. It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the teachings of Chan with the teachings of Naruse in order to select the proper bits to be used for a given scan (column 7, lines 16-18).

17. With respect to claims 3, 5, and 7, Naruse does not disclose a code generator further comprising bit reordering means, coupled to the output of said counter, for receiving each M-bit count, whereby the M-bit counts are ordered from least significant bit to most significant bit, and whereby the bit reordering means reorders the bits from most significant bit to least significant bit.

Chan discloses a code generator further comprising bit reordering means, coupled to the output of said counter, for receiving each M-bit count, whereby the M-bit counts are ordered from least significant bit to most significant bit, and whereby the bit reordering means reorders the bits from most significant bit to least significant bit (Figure 10).

18. The motivation for combining the teachings of Chan with Naruse has been disclosed above.

19. With respect to claim 8, Naruse does not disclose a code generator further comprising a switch coupled to said bit reordering means, whereby when the switch is in a first position, the bit reordering means is coupled to the output of said counter to reorder the bits of said binary number, and when the switch is in a second position, the bit reordering means is decoupled from the output of said counter and the bits of said binary number are not reordered.
Chan discloses a code generator further comprising a switch coupled to said bit reordering means, whereby when the switch is in a first position, the bit reordering means is coupled to the output of said counter to reorder the bits of said binary number, and when the switch is in a second position, the bit reordering means is decoupled from the output of said counter and the bits of said binary number are not reordered (column 6, lines 64-67 through column 7, lines 1-24).

20. It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the teachings of Chan with the teachings of Naruse in order to select the proper bits to be used for a given scan (column 7, lines 16-18).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ramya Ananthanarayanan whose telephone number is (571) 272-5860. The examiner can normally be reached on Monday through Friday, 8:30 -5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RA

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SUPERVISORY PATENT EXAMINER
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